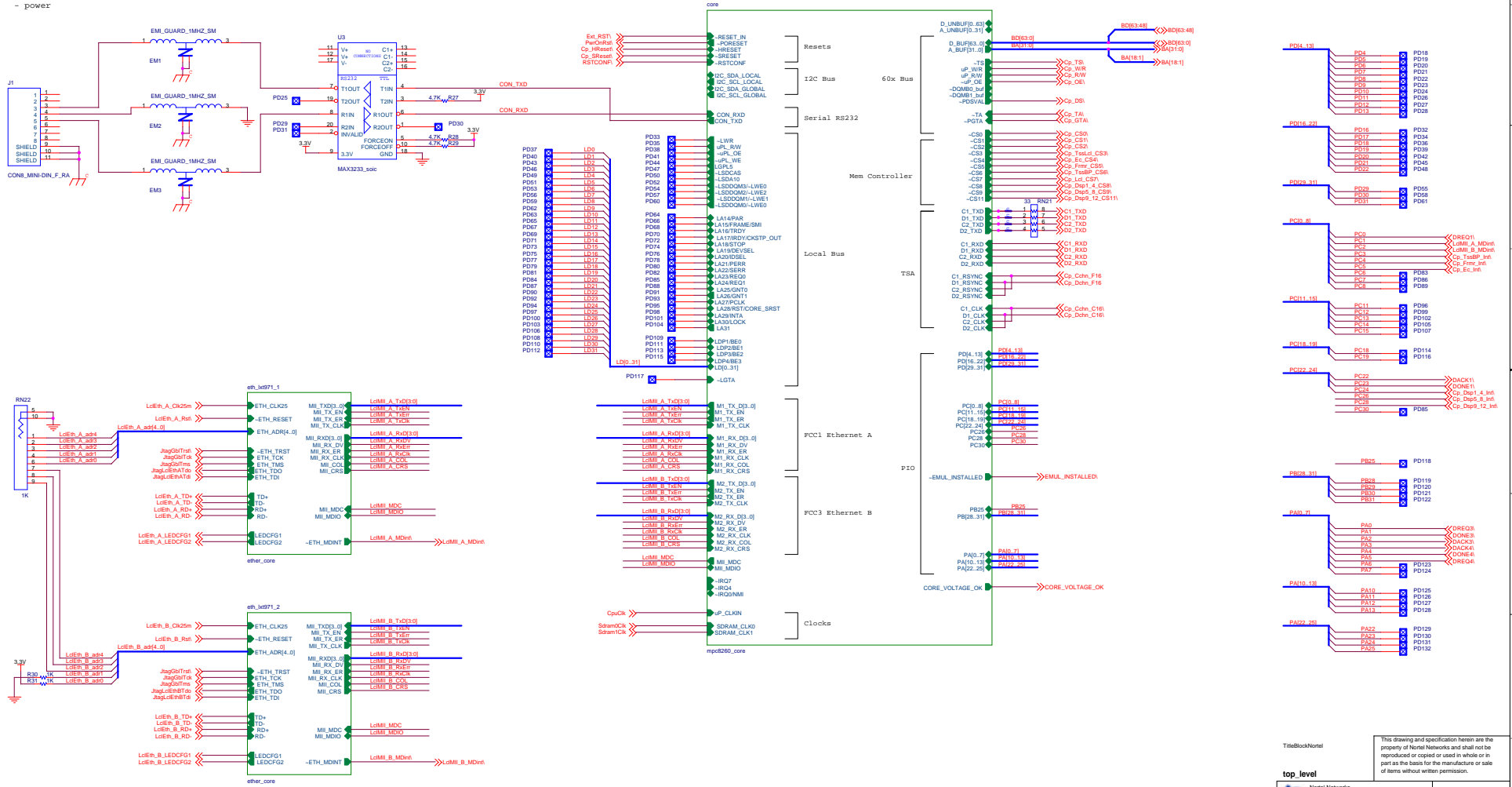


HIERARCHAL CORE BLOCK INCLUDES

- S260
- SDRAM
- ROM
- dual ETHER
- adr/data buffer
- I2C local
- console
- RESET
- emulator/jtag tester
- power

Letter	Zone	Description	Date	By	Approved



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top_level

Nortel Networks
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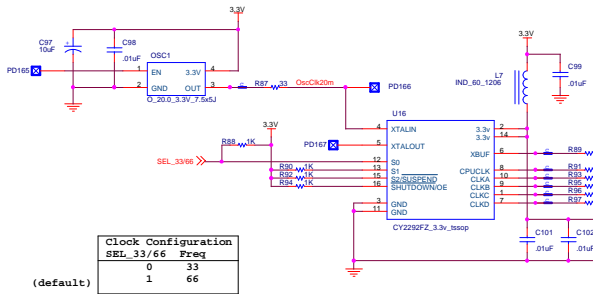
cTMS-1000

Size: Document Number: **cTMS-1000**

Date: Thursday, February 29, 2001 Sheet 1 of 33

Document File Name: L:\MIB\TOPLEVEL\REV1_TCM1000.DWG

mpc8260_core



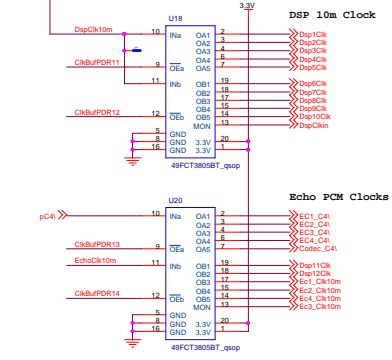
Clock Configuration		
SEL	33	Freq
(default)	0	33
	1	66

60 ohm Impedance Match for
CY2292FZ output clocks

28 ohm Impedance Match for
49FCT3805 output clocks

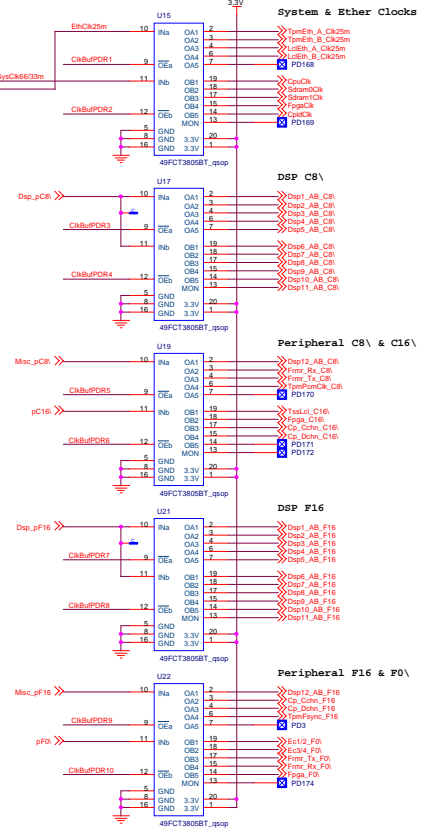
System Clocks trace lengths
must NOT exceed 2.5in

Dsp and Echo Clks trace lengths
must NOT exceed 3.0in.



DSP 10m Clock

Echo PCM Clocks



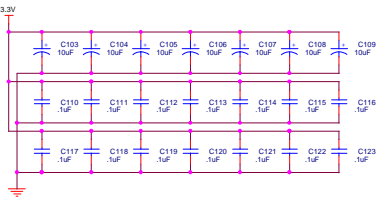
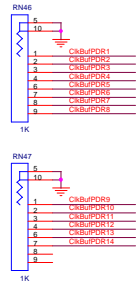
System & Other Clocks

DSP C8\

Peripheral C8\ & C16\

DSP F16

Peripheral F16 & F0\



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APPROVED:

Doc: CTMS-1000

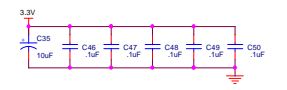
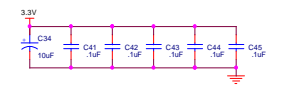
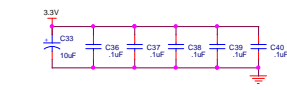
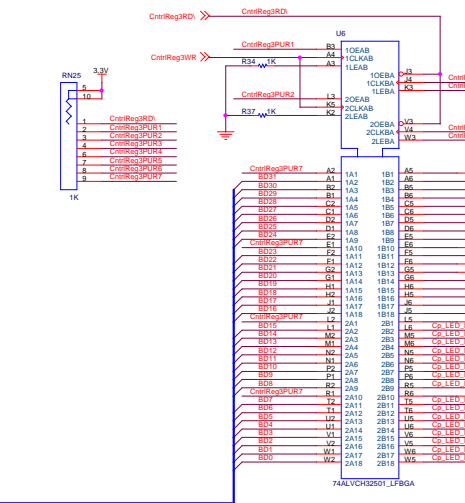
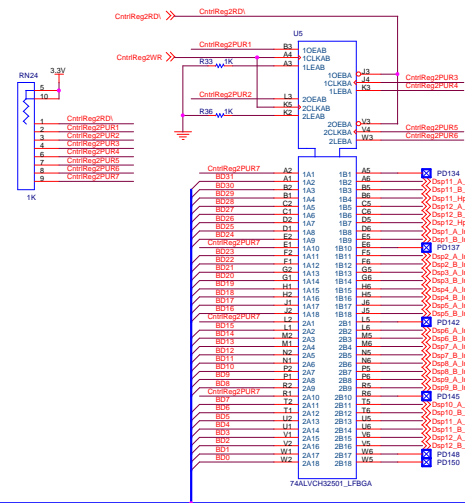
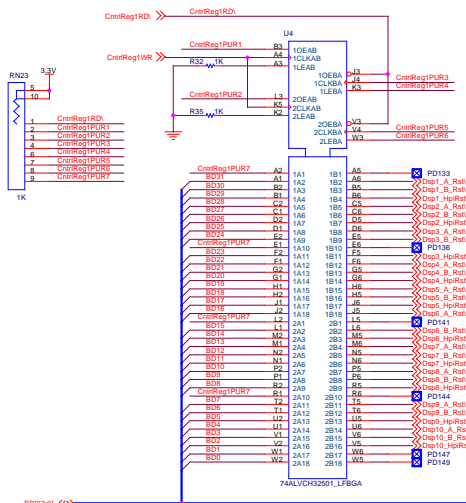
Rev: 1

Date: Thursday, February 27, 2003

Page: 2 of 33

Document File Name: C:\ENR\10000202\AVR\CTM110001.DWG

clocks



Span LEDs
PCI GeoAdr
CT Bus GeoAdr

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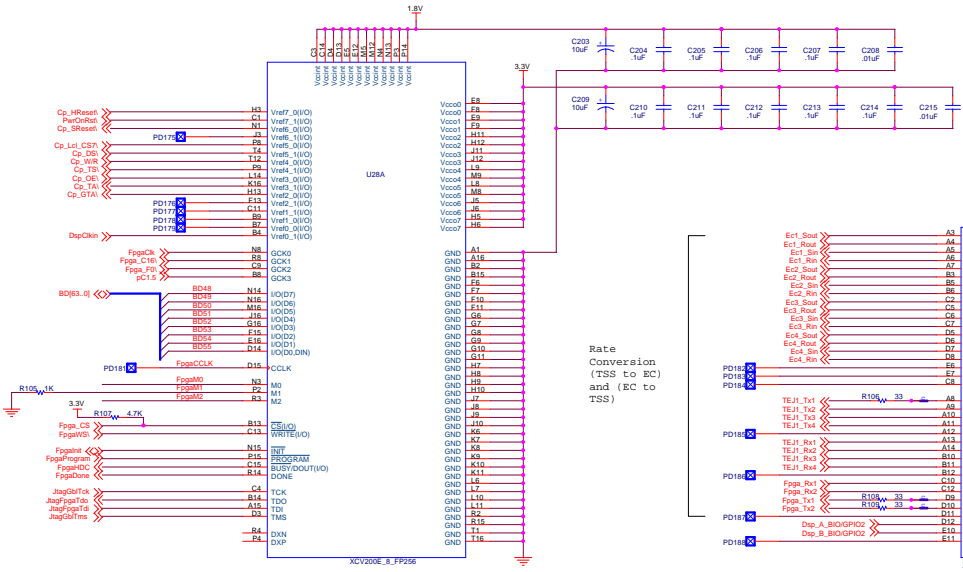
Nortel Networks
4000 Veterans Memorial Highway
Bohemia, NY 11716

APPROVED:

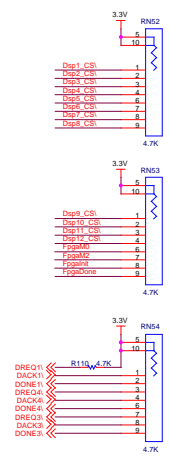
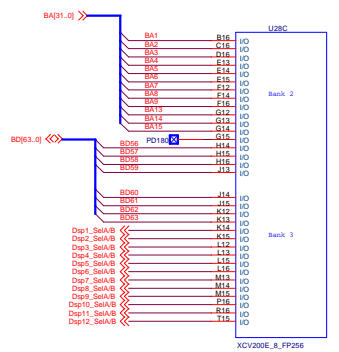
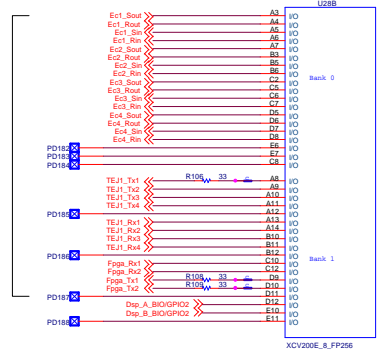
cTMS-1000

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Rev: 1

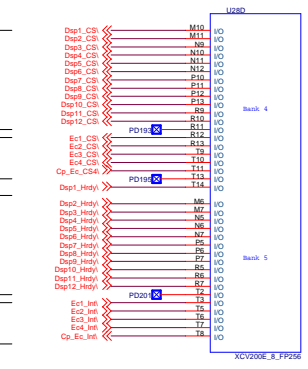


Rate Conversion (TSS to EC) and (EC to TSS)

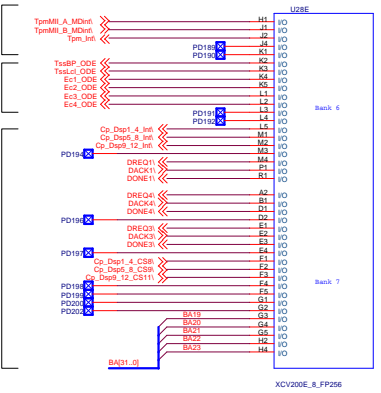


Base Addr for E01 = 0A001000'h
 Base Addr for E02 = 0A002000'h
 Base Addr for E03 = 0A003000'h
 Base Addr for E04 = 0A004000'h

DSP HPI Chip Selects
 Echo CSs
 DSP HPI Ready
 Hrdy\ used to Return TA\ to uP
 Interrupts from Echo



TPM Interrupt
 Echo, TssClc1, TssBp ODE
 DSP Control

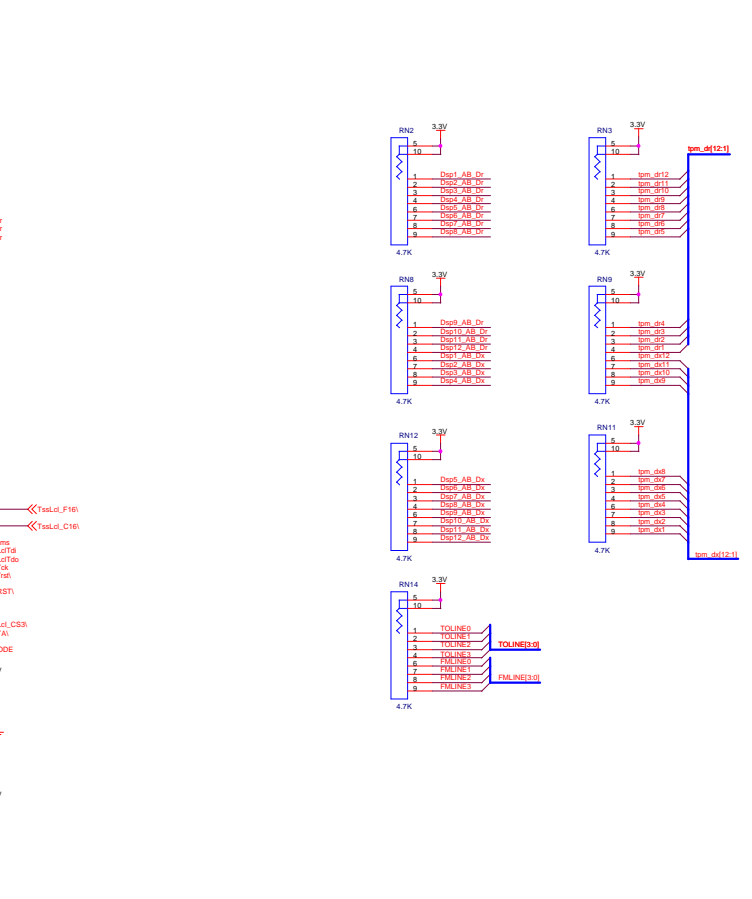
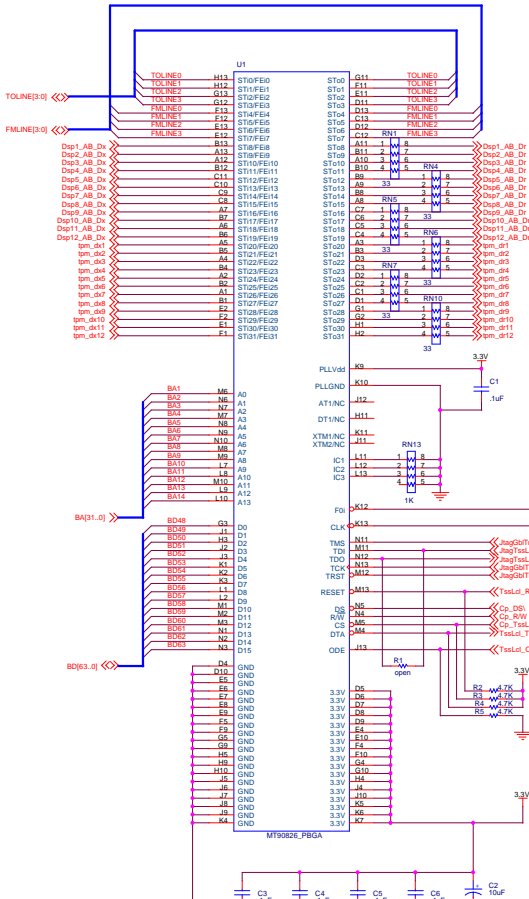


TimeBookNortel

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top_level		APPROVED:	
Nortel Networks 4000 Veterans Memorial Highway Bohemia, NY 11716			
File	cTMS-1000		
Size	Document Number	Sheet	Rev
Created/Date	Thursday, February 22, 2001	of	33
Date	Thursday, February 22, 2001	of	33
Document File Name	c:\c\1000\2001\FEBRUARY\FEB_22_01\F256_001.DSN		





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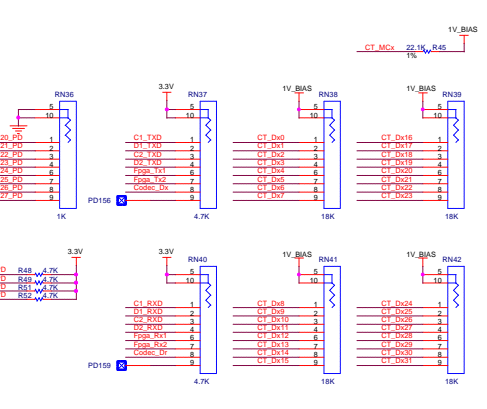
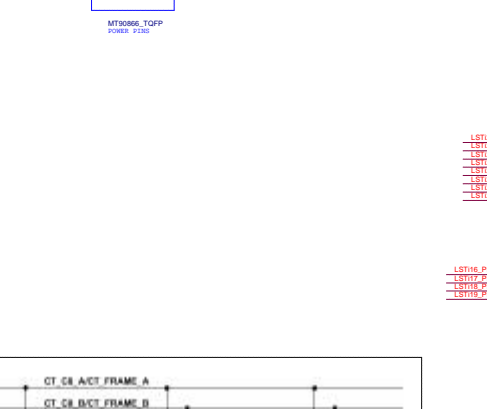
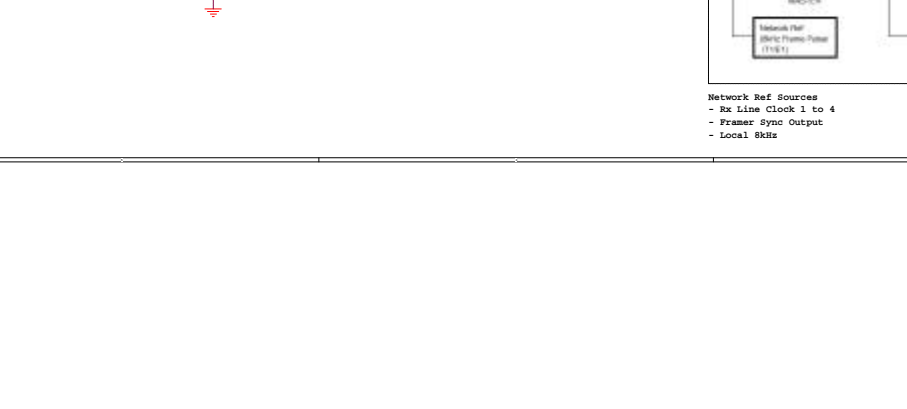
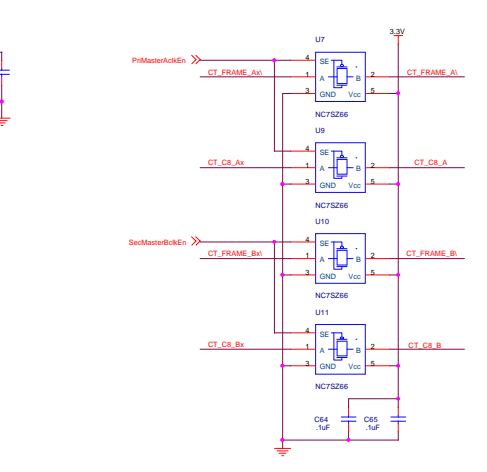
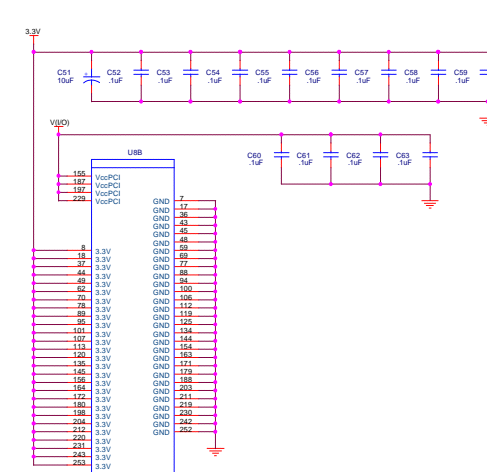
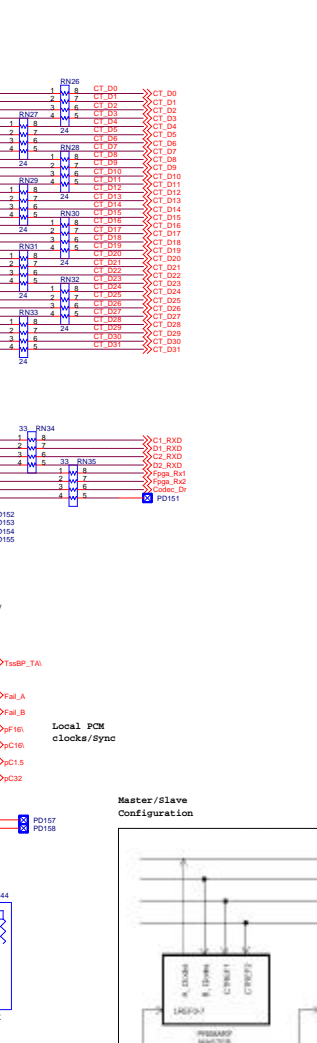
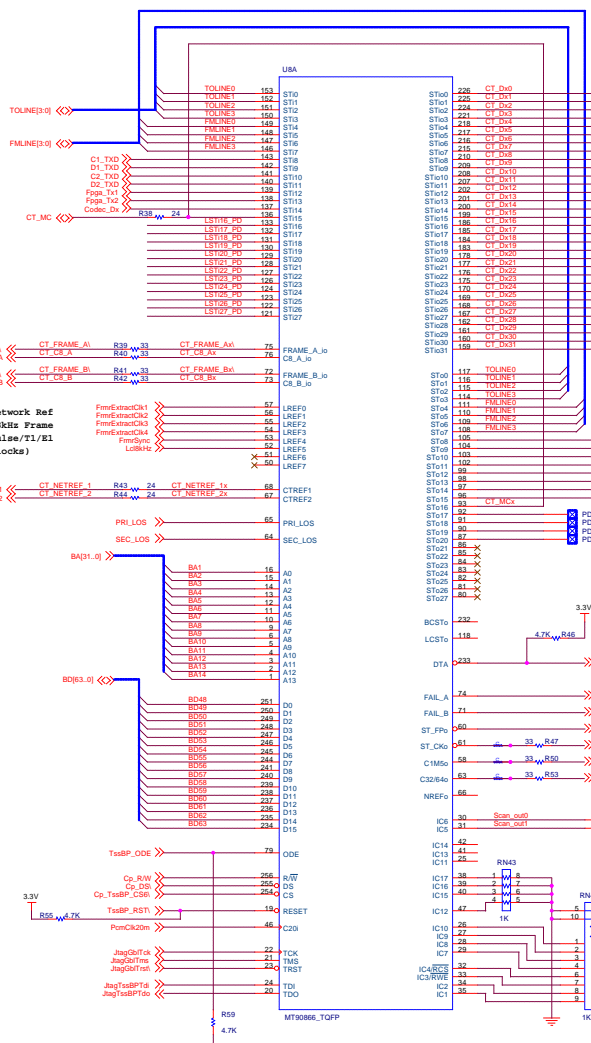
Nortel Networks
4000 Veterans Memorial Highway
Basking Ridge, NJ 11716

APPROVED:

Size: cTMS-1000
Date: Thursday, February 22, 2001
Document File Name: L:\C:\MSD\WORK\2001\TMS1000.DWG

Sheet	6	of	33
Rev	1		

t.s.s

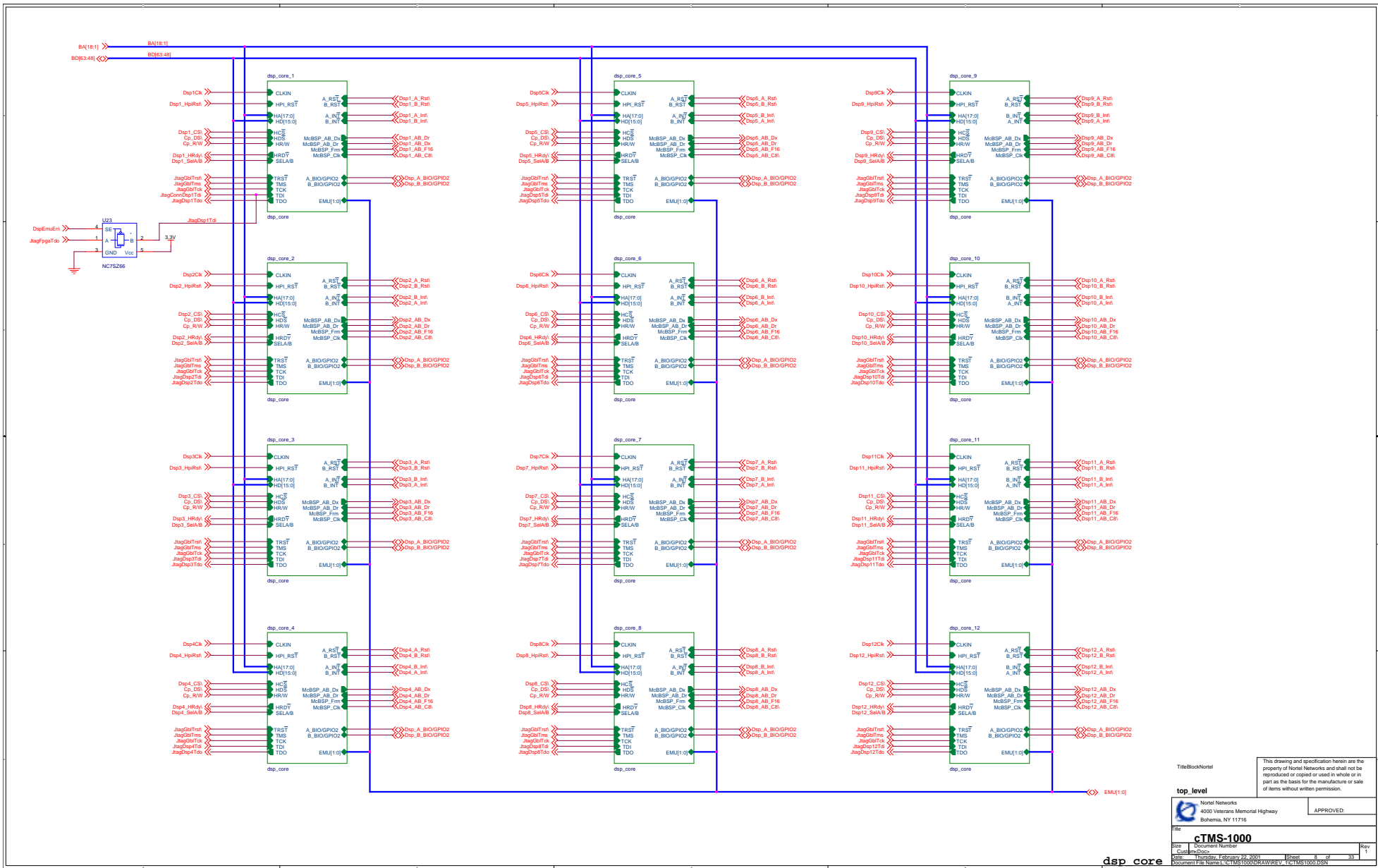


Network Ref Sources
 - Rx Line Clock 1 to 4
 - Frame Sync Output
 - Local Khz

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cTMS-1000	
Size	Document Number
Sheet	Thursday, February 22, 2001
Document File Name	L:\C:\MSD\1000\REV0001\REV0001.TMS1000.DWG

H.110 interface

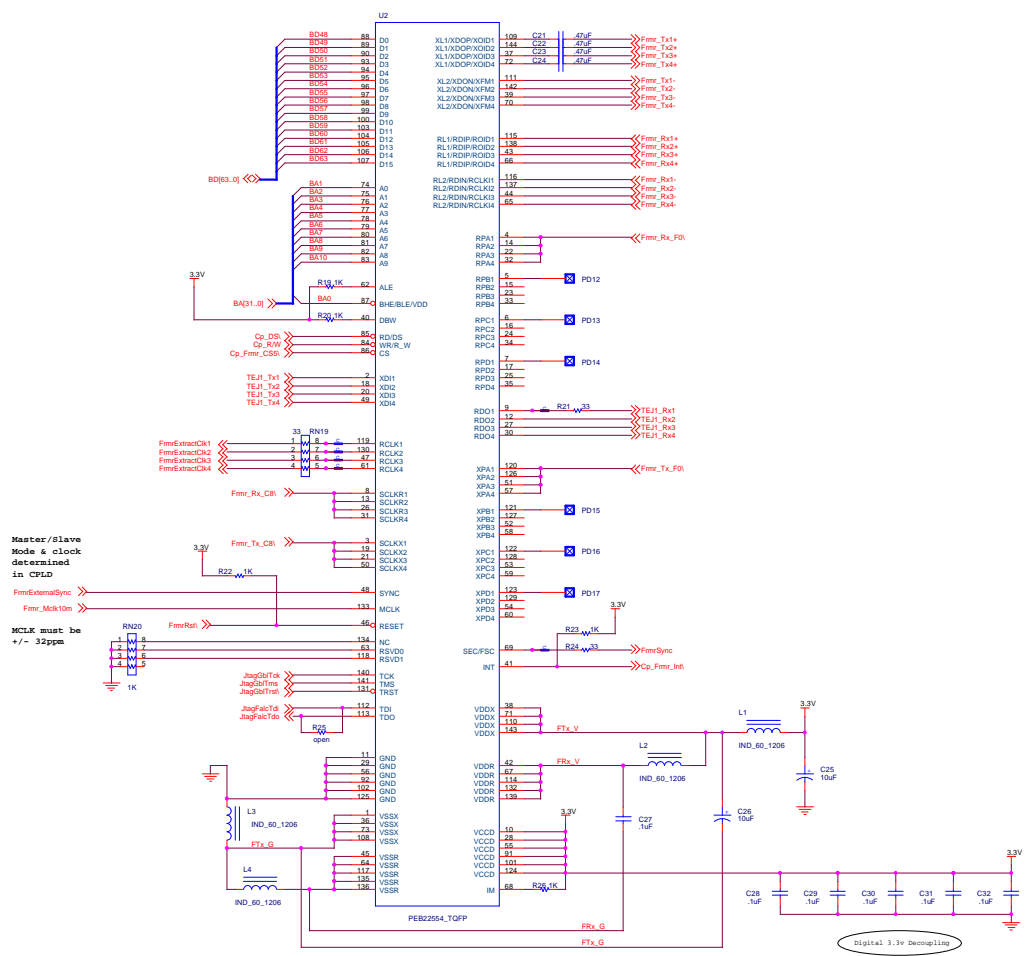


TitleBlockNonsel
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 Noriel Networks
 4000 Veterans Memorial Highway
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Size	Document Number	Sheet	1
Created	Tuesday, February 23, 2001	8	33
File Name	C:\TMS1000\DRAWING - TC:TMS1000.DSN		

dsp_core



Master/slave Mode & clock determined in CPLD

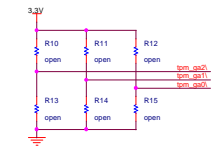
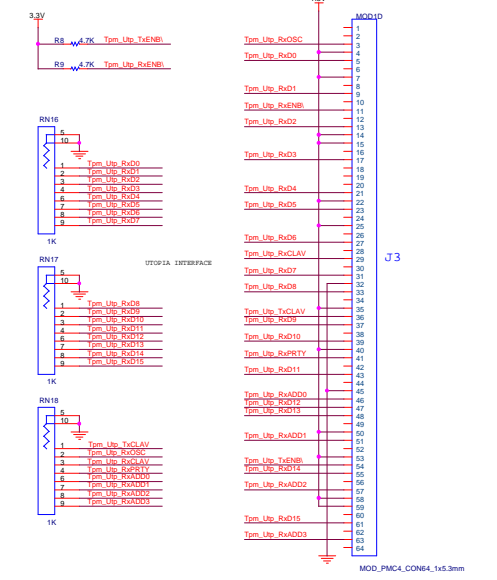
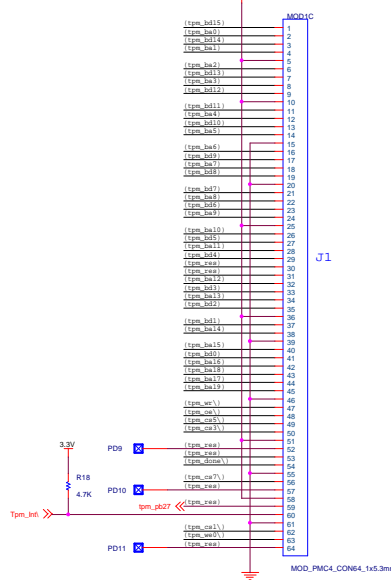
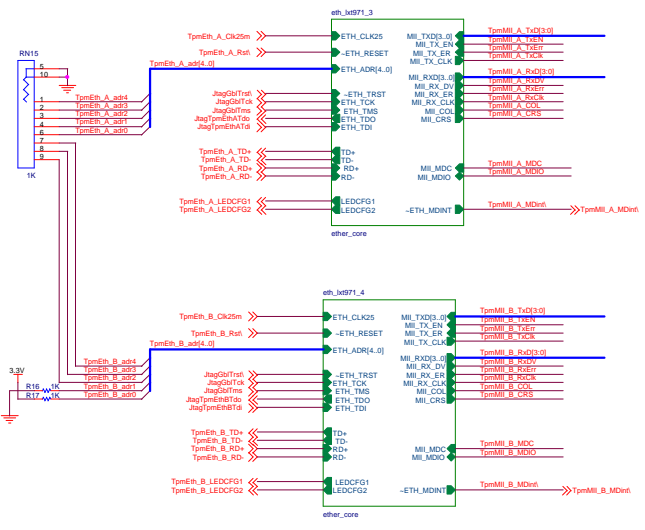
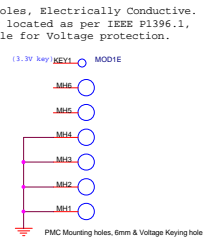
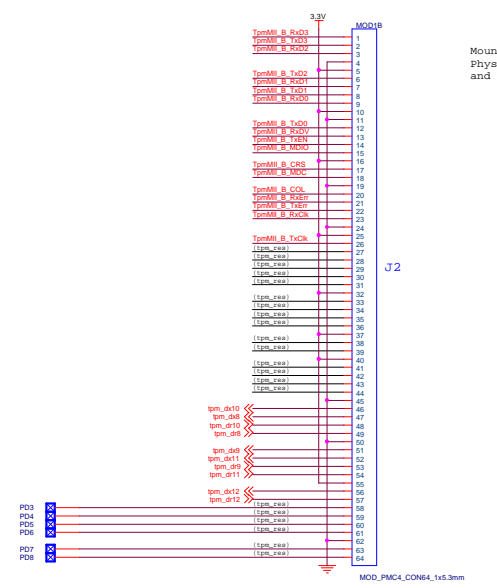
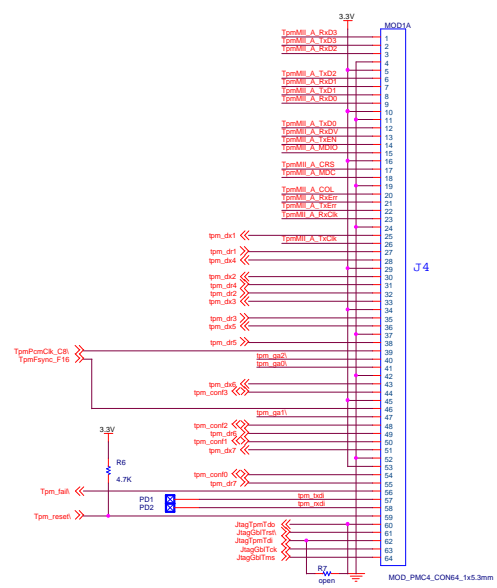
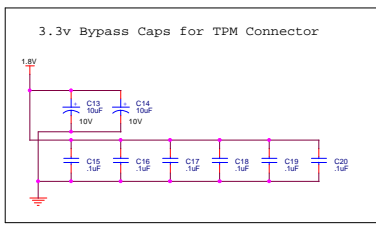
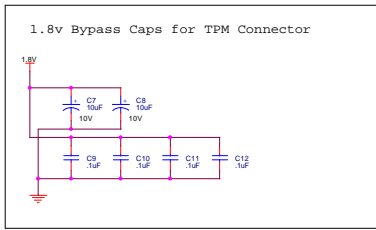
FmR_ExtMck10m

MCLK must be +/- 32ppm

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cTMS-1000 Size: Document Number Date: Thursday, February 22, 2001 Document File Name: L:\cTMS\1000\REV0001_TQFP.TMS1000.DWG		
Sheet	10 of 33	Rev 1

quad framer



TableBookNotes

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top level

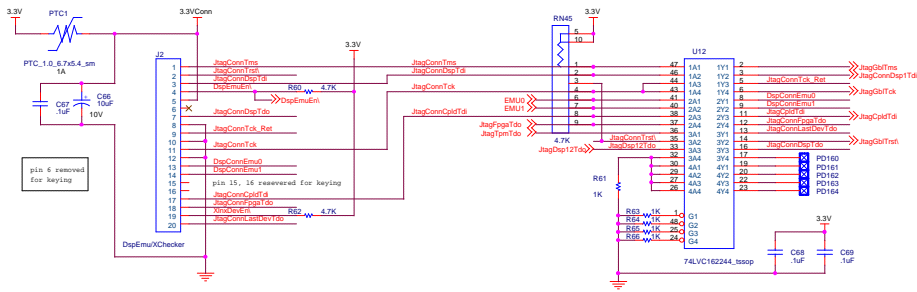
Nortel Networks
4000 Veterans Memorial Highway
Basking Ridge, NJ 07170

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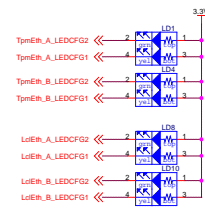
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Date: Thursday, February 22, 2001
Sheet: 11 of 33
Document File Name: L:\C:\MSD\WORK\WV01-TEL\TMS1000.DWG

tpm interface

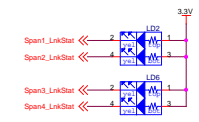
DSP Emulator/JTAG Test
/Xilinx JTAG
Connector



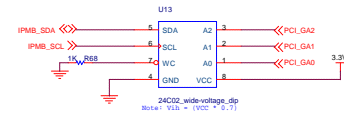
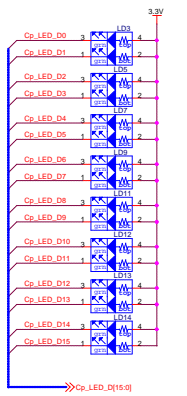
Ethernet LEDs



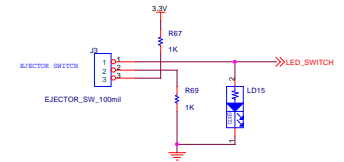
TEJ1 Span Status LEDs



Diagnostic LEDs

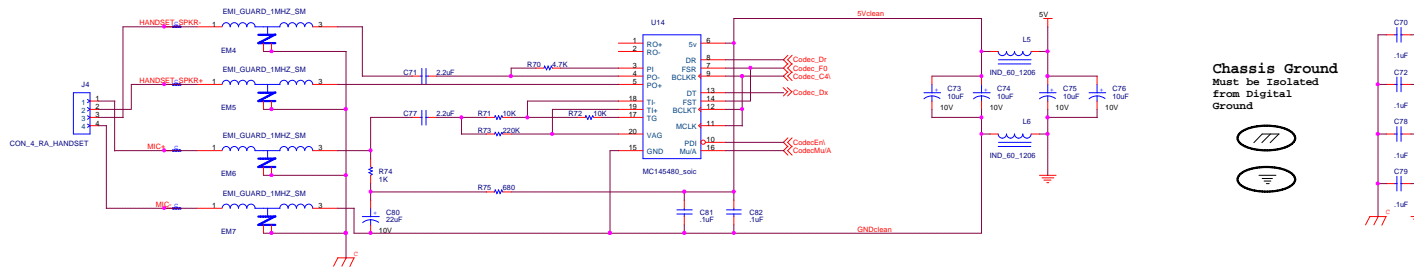


I2C peripheral slot



Track 5Vclean & GNDclean

Telephone
Handset
w/Record
In



Chassis Ground
Must be Isolated
from Digital
Ground



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top level

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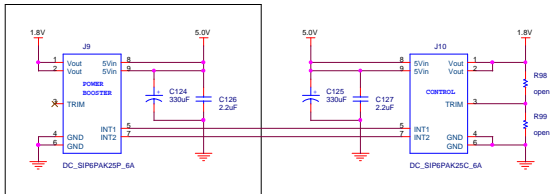
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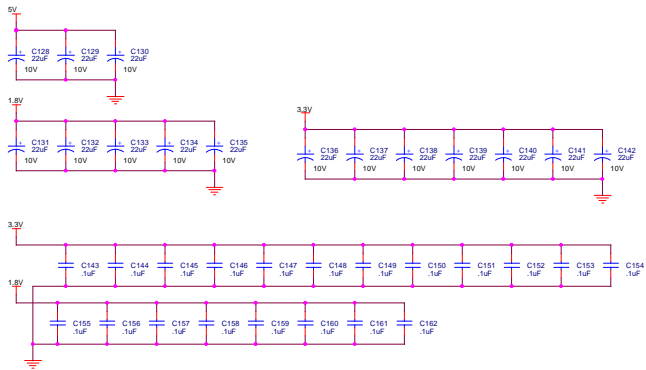
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Sheet	Sheet	1
Date	Thursday, February 22, 2001	Sheet 13 of 33
Document File Name	L:\cTMS\1000\REV0001\REV0001_TEL1RST000.DWG	

diagnostics

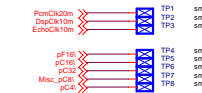
+1.8V Generation



Install only if TPM-800 Option Card is installed



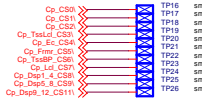
PCM/Peripheral Clocks



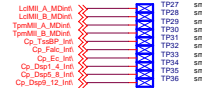
60x Bus Controls



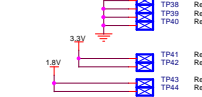
Chip Selects



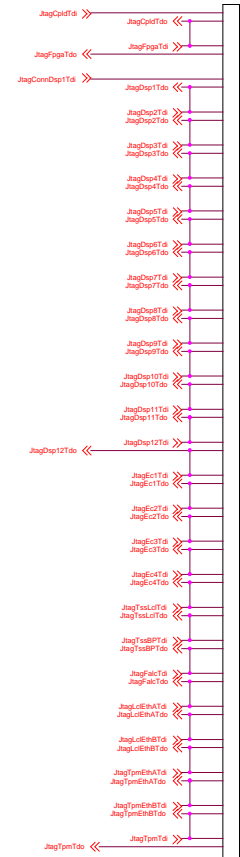
Interrupts



Power



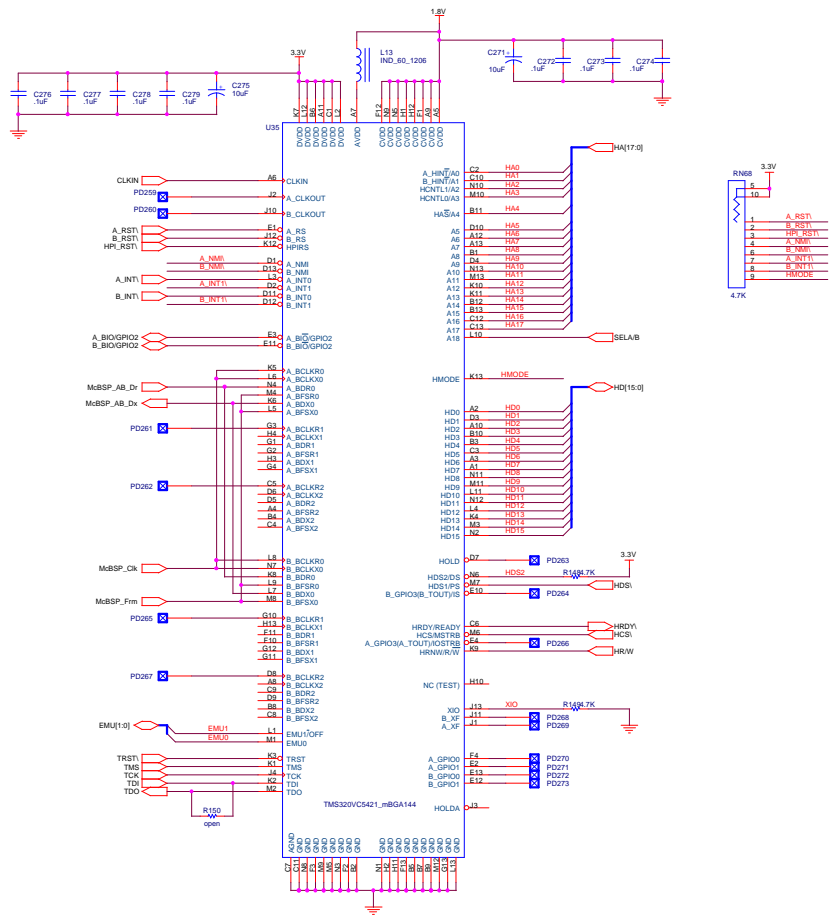
JTAG Test/Dep Emulator/FPGA programming Chain



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Nortel Networks 4000 Veterans Memorial Highway Basking Ridge, NJ 07005		APPROVED:
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Size	Document Number	Rev
Sheet	PCB Layout	1
Date	Thursday, February 22, 2001	Sheet 14 of 33
Document File Name: L:\CTMS-1000\REV0001\TOP_LEVEL1000.DWG		

caps pwr tps



dsp_core_1\TitleBlock\Nortel

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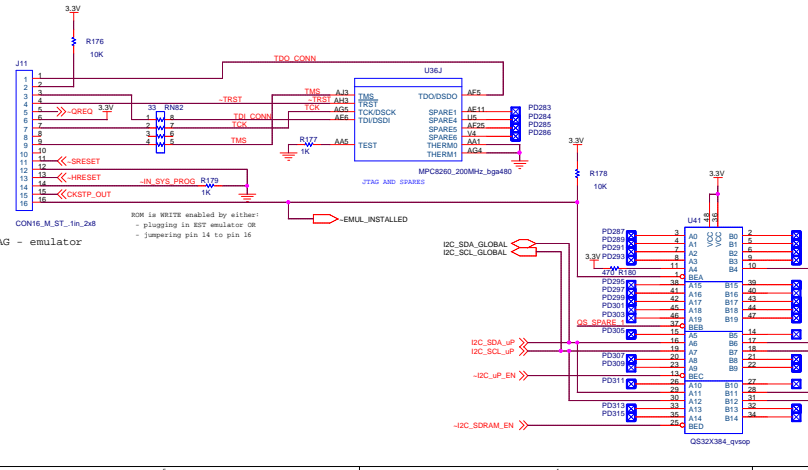
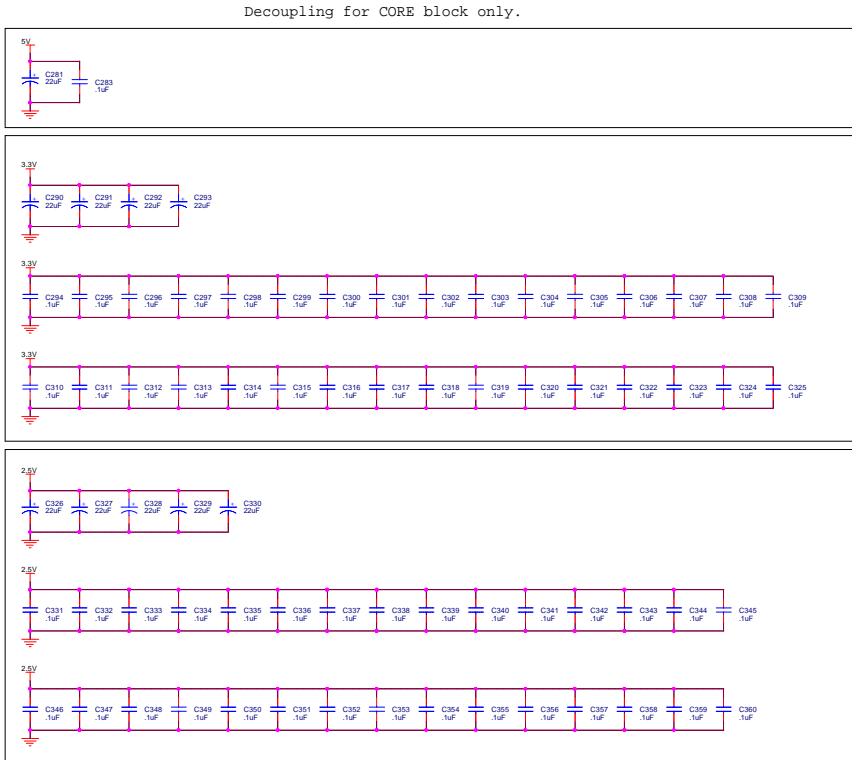
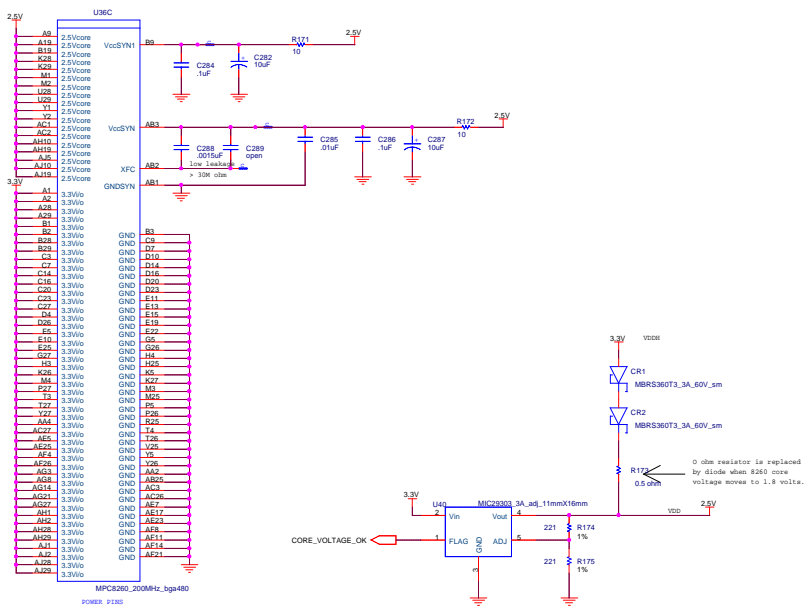
dsp_core

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4000 Veterans Memorial Highway
Bohemia, NY 11716

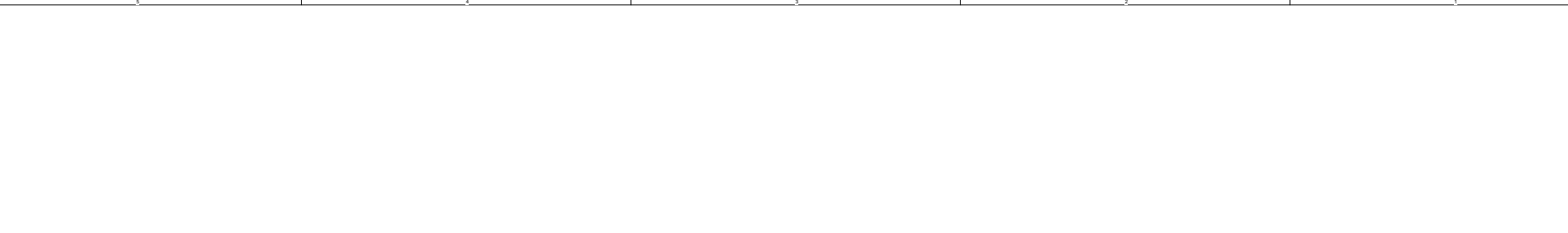
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Size	Document Number	1
Callend/Doc		
Date	Thursday, February 22, 2001	Sheet 18 of 33
Document File Name	L:\cvt\5420\cvt\5420_144\TMS1000.DWG	

tms3205421



8260 Decoupling			
3.3V		2.5V	
qty	size	qty	size
9	0.1uF	23	0.1uF
1	10uF	2	10uF



coreTitleBlockNonel

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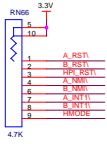
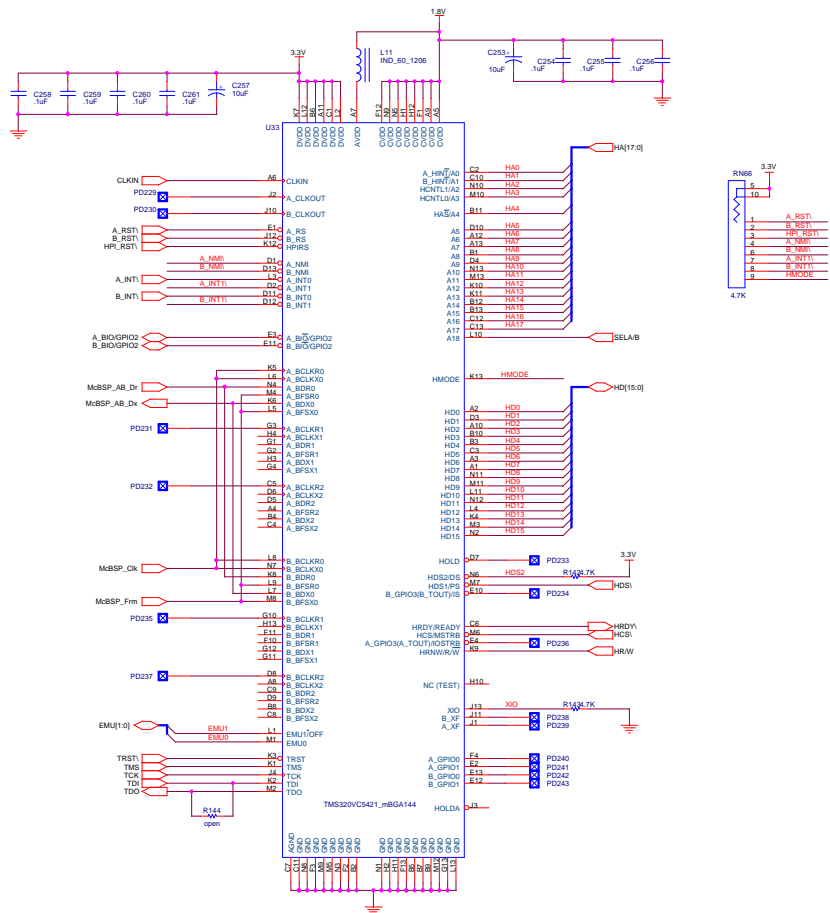
mpc8260_core

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Bohemia, NY 11716

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File: cTMS-1000
Document Number: 4800
Date: Thursday, February 22, 2000
Sheet: 11 of 31
Rev: 1

misc



dsp_core_2/TitledBookNortel

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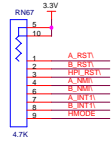
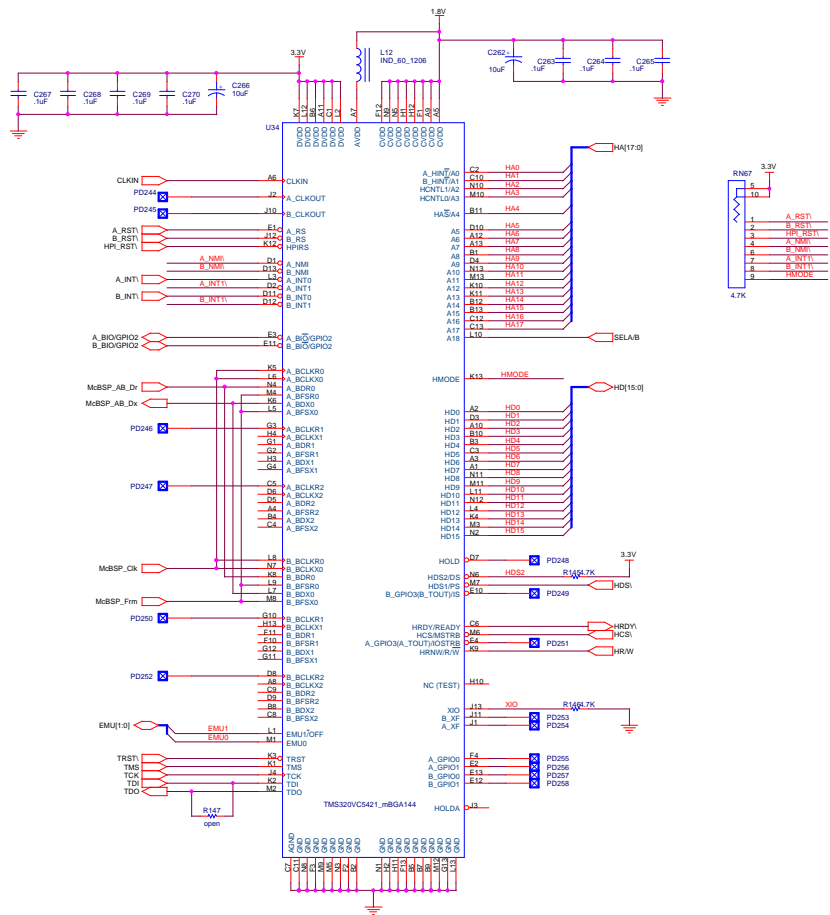
dsp_core

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 Bohemia, NY 11716

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Full	Thursday, February 22, 2001	19 of 33	1
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tms3205421

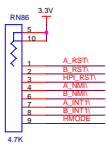
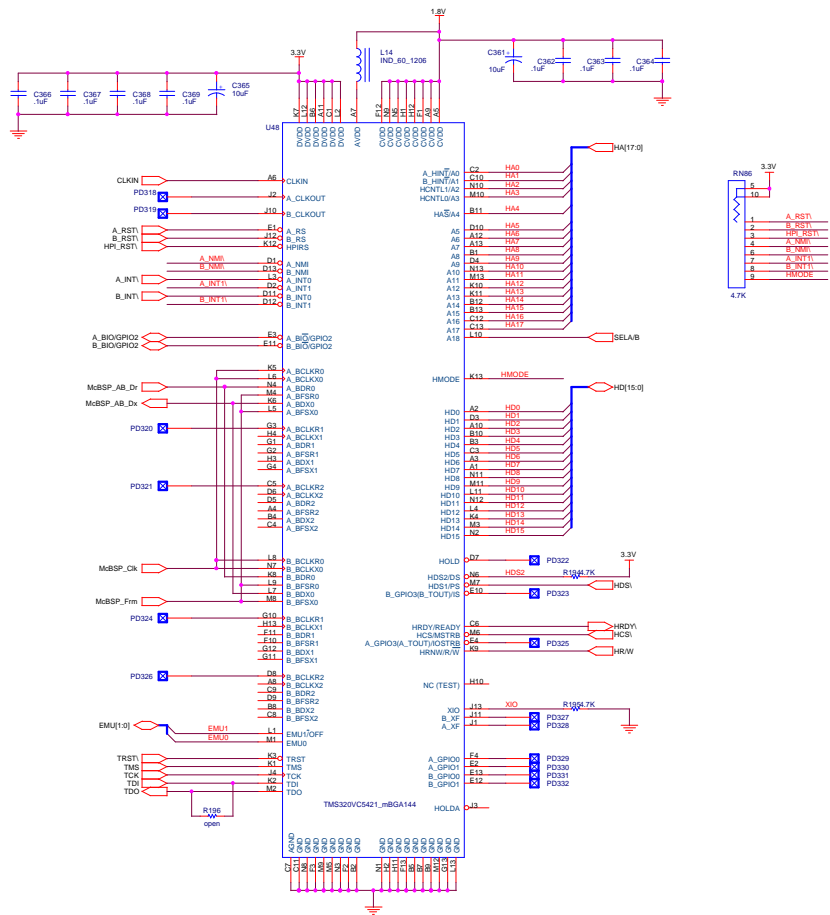


dsp_core_3JTitleBlockNortel

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dsp_core Nortel Networks 4000 Veterans Memorial Highway Bohemia, NY 11716		APPROVED:
cTMS-1000		
Size	Document Number	Rev
Path	Thursday, February 22, 2001	Sheet 20 of 33
Document File Name: L:\cTMS\1000\cTMS1000_3J_TITL1000.DWG		

tms3205421



dsp_core_47TitleBlockNortel

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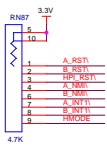
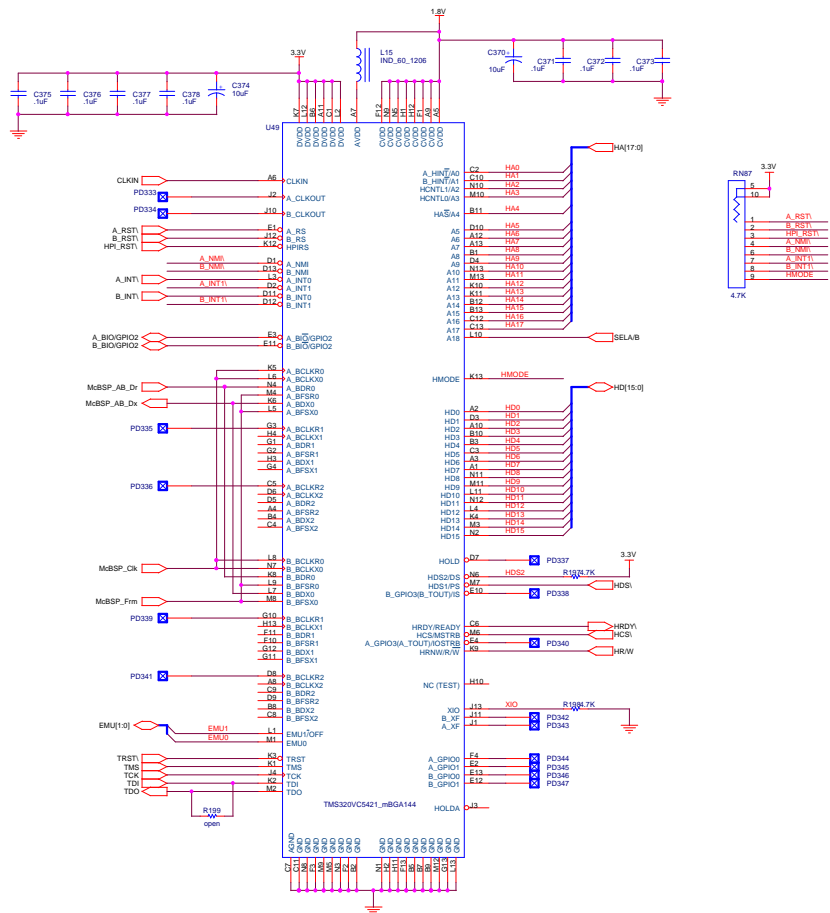
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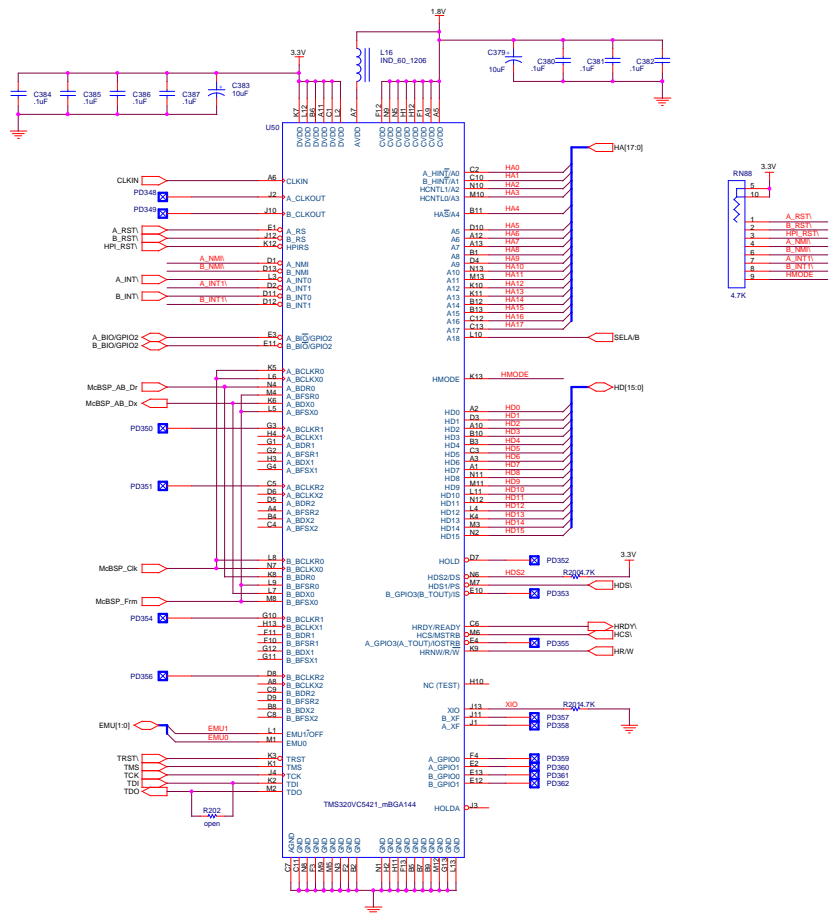


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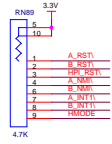
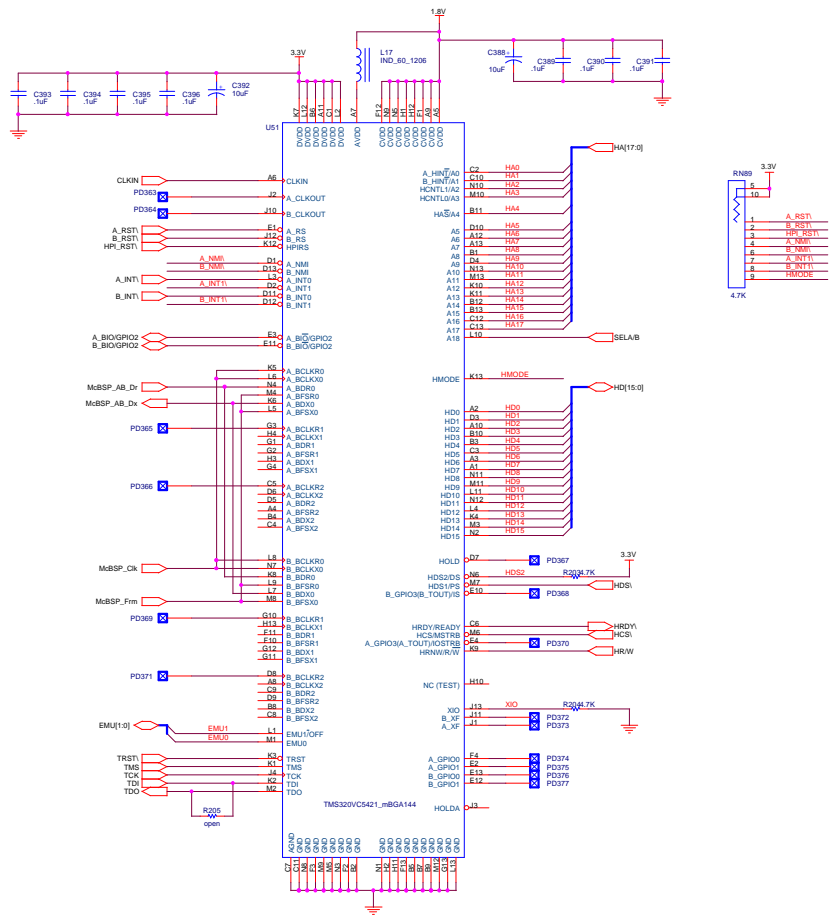


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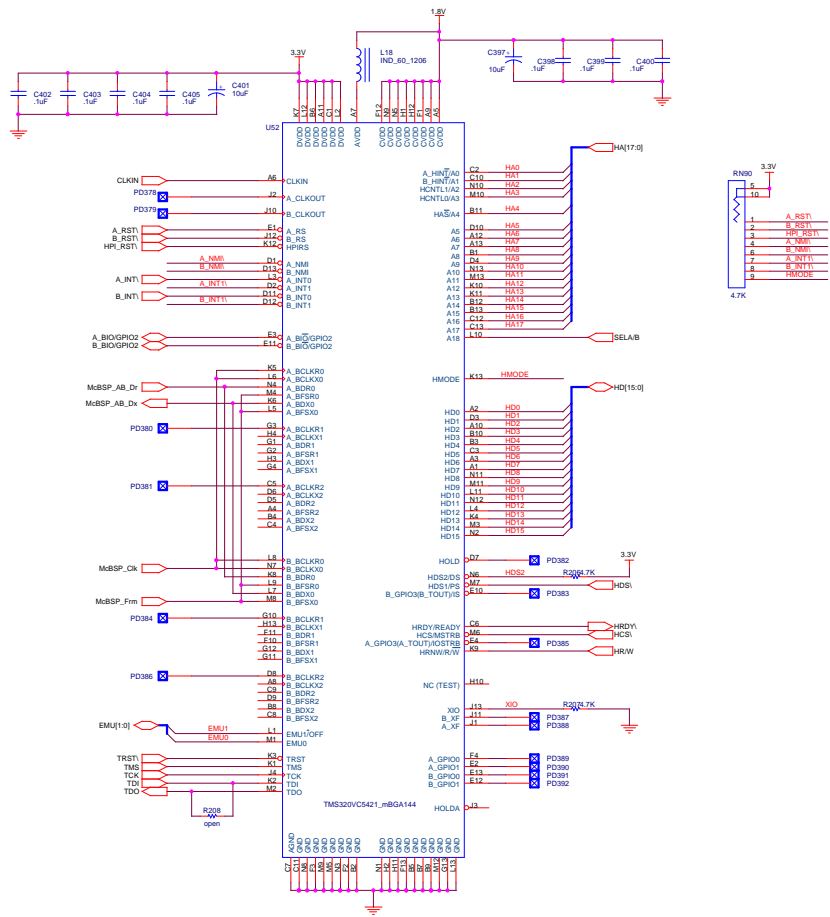


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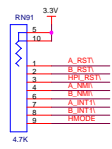
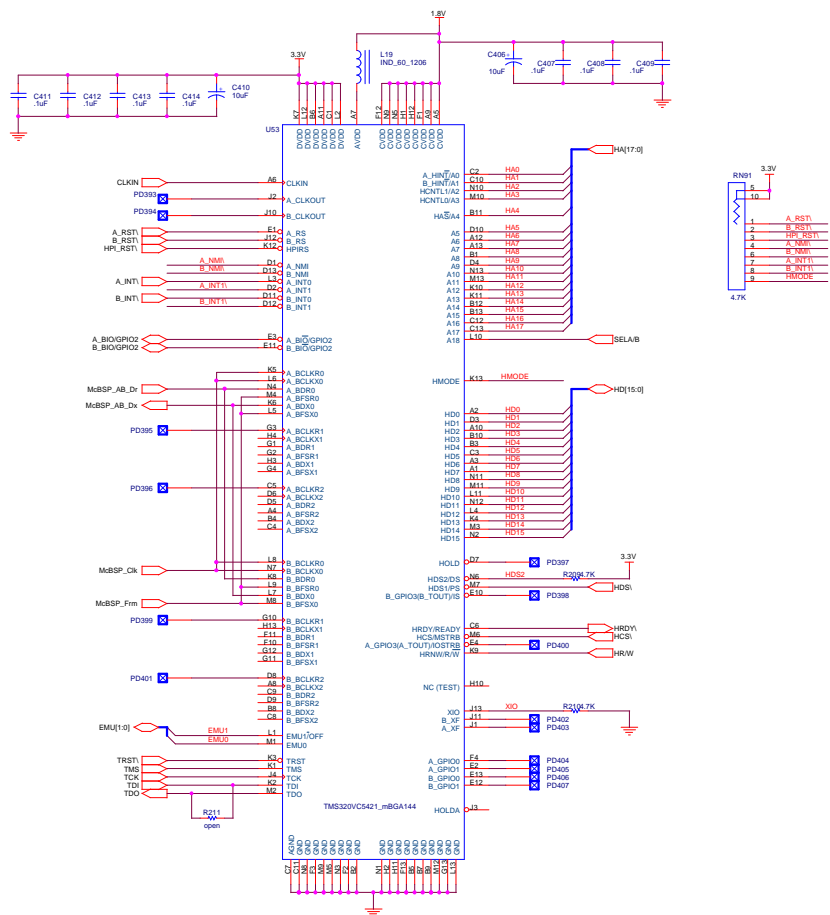


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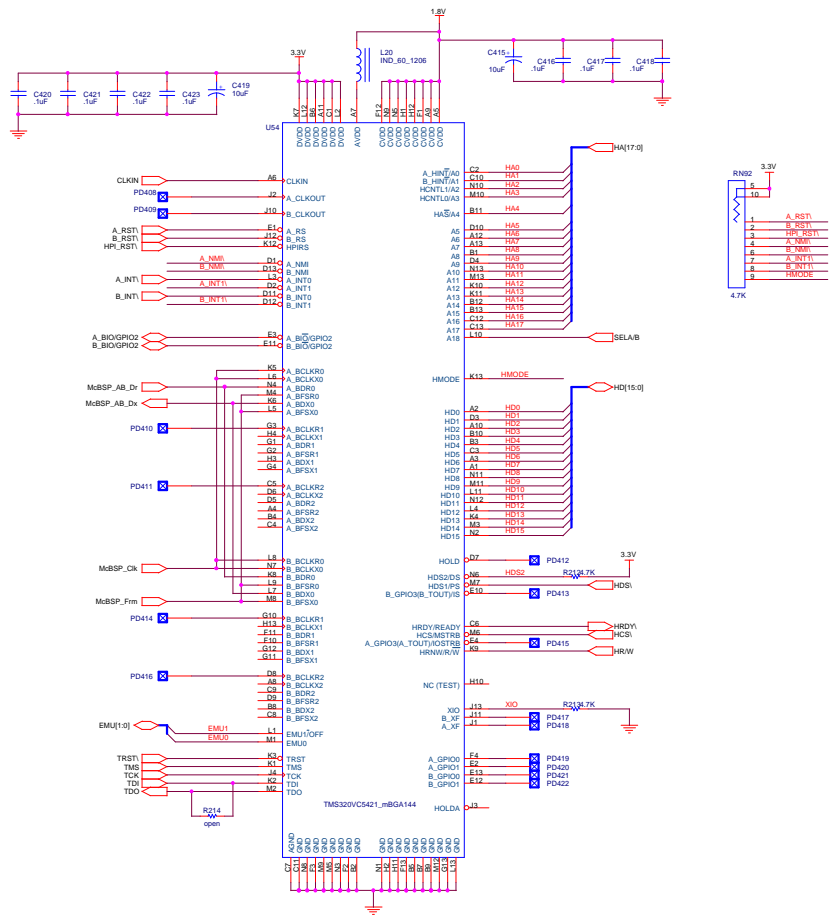
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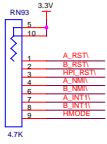
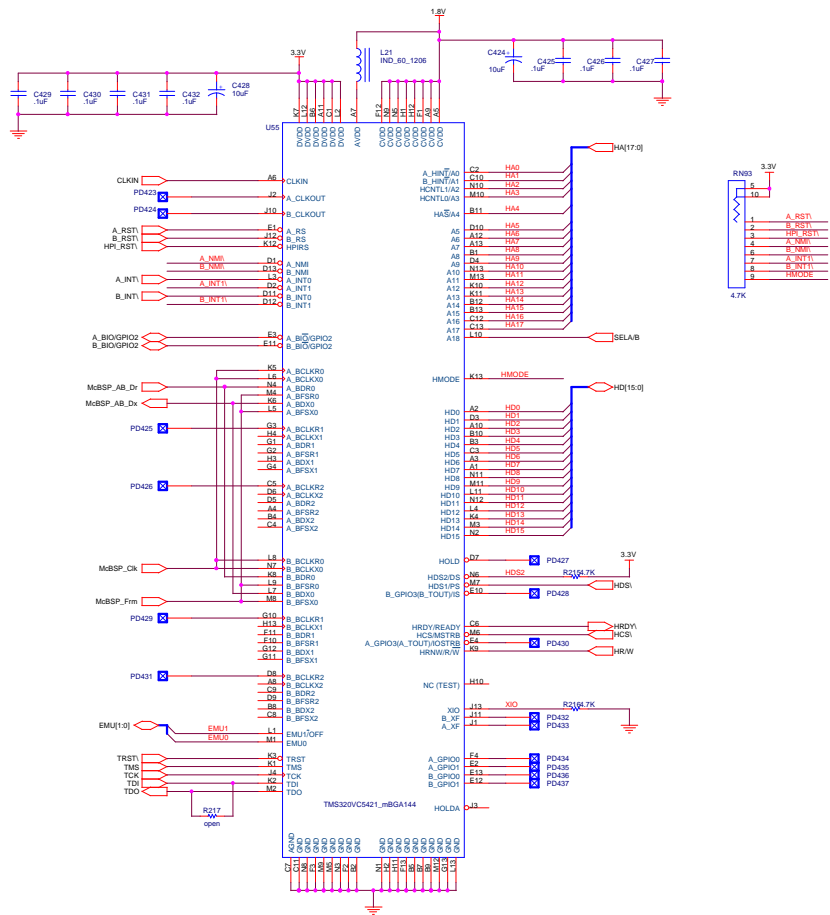


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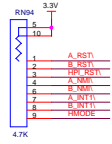
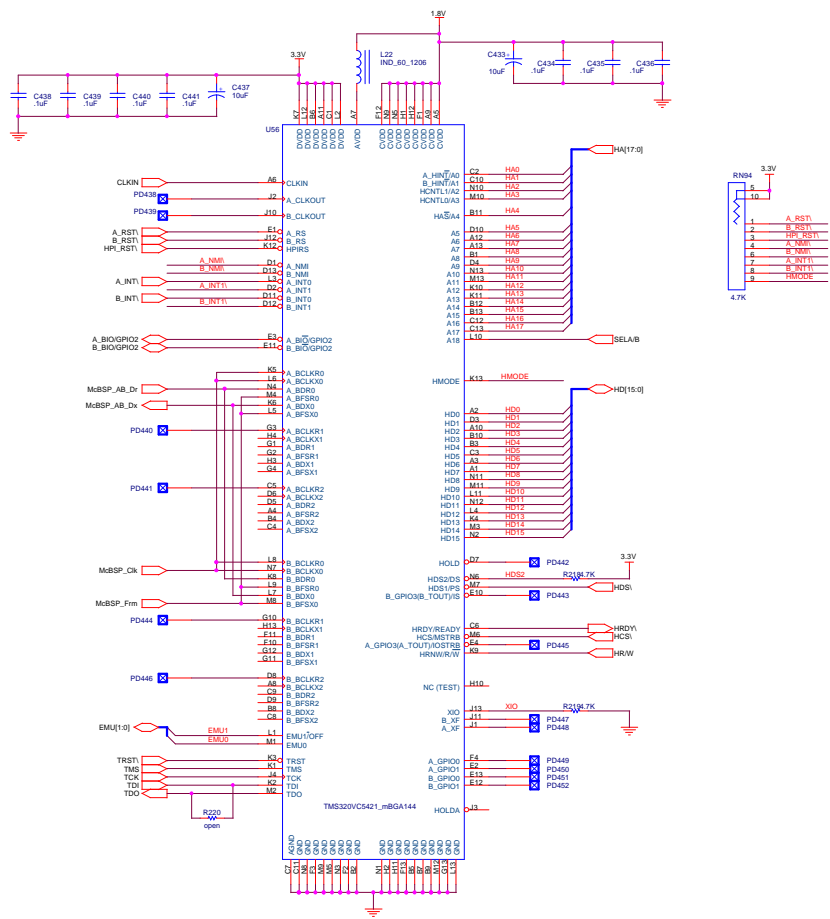


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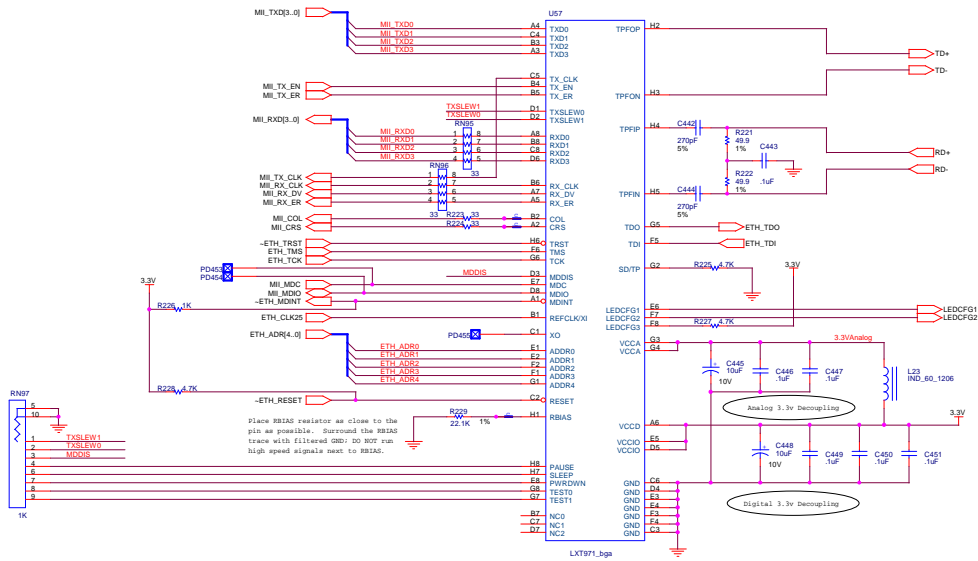
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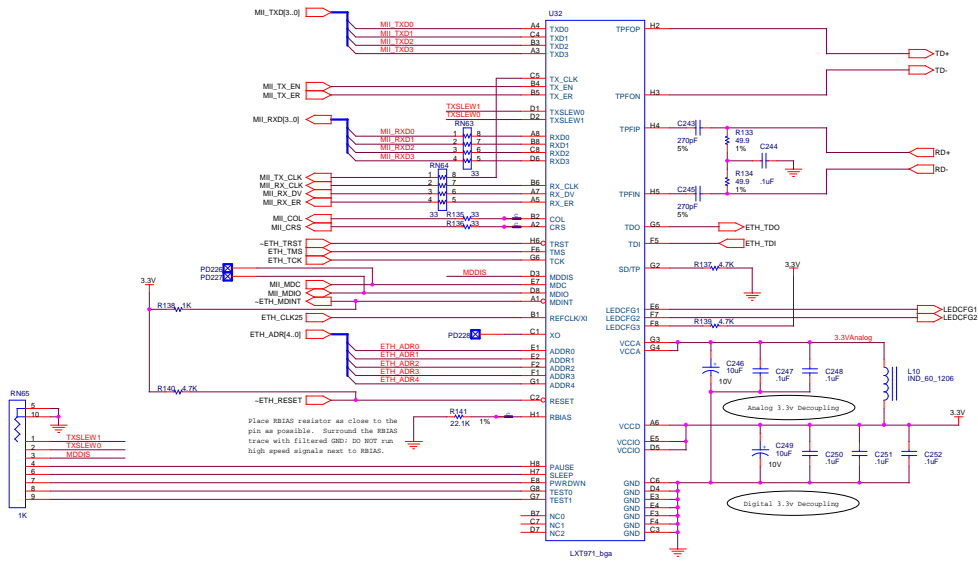
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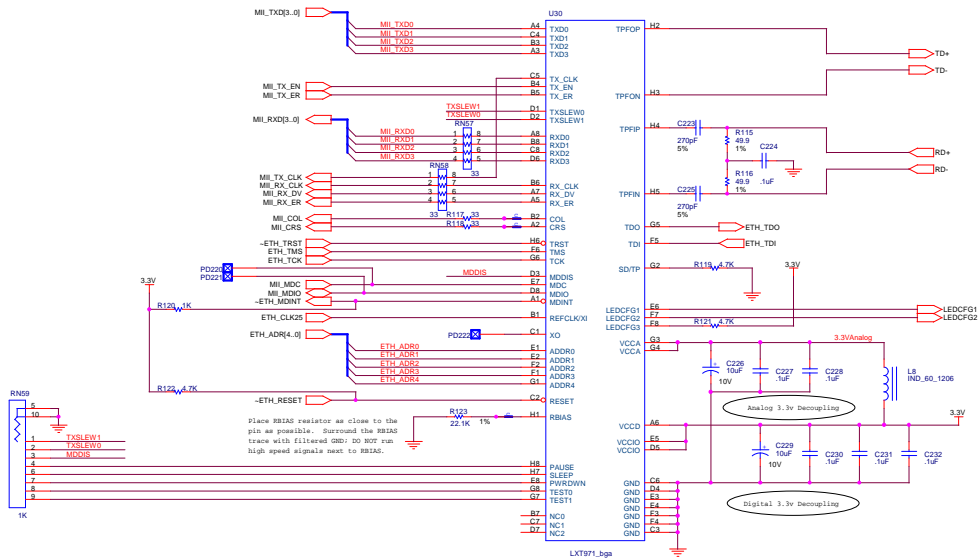
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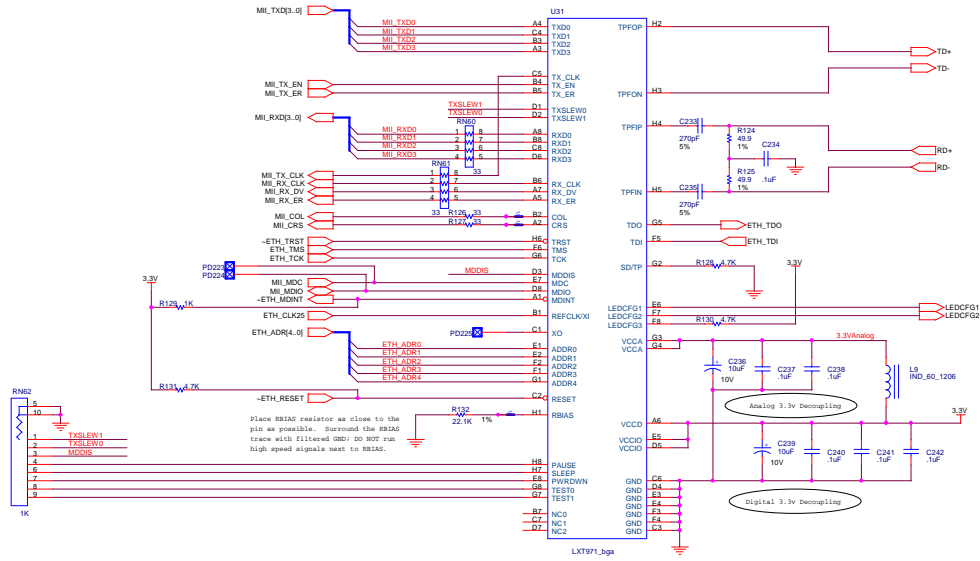
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